REMARKS

Claims 1, 14, 19, and 24 are currently amended. Claims 29 and 32-40 are canceled. Claims 32-40 correspond to non-elected subject matter, and Applicant reserves the right to file one or more divisional applications for the non-elected subject matter. The Specification has been amended to correct a typographical error. Applicant respectfully submits that the amendments contained herein are fully supported by the Specification as originally filed and do not contain new matter.

Election/Restriction

Undersigned Patent Agent Tod A. Myrum provisionally elected Group I, claims 1-28 and 30-31, for prosecution without traverse during a telephonic interview with Examiner Sheng Jen Tsai on April 24, 2006. Affirmation of this election is made herewith.

Claim Objections

Claim 29 was canceled in response to the Examiner's statement regarding missing claim 29.

Claim Rejections Under 35 U.S.C. § 102

Claims 1-4, 6-8, 11, 13-15, 17-20, and 22-23 were rejected under 35 U.S.C. § 102(b) as being anticipated by Robinson (U.S. Patent No. 5,937,423). Claims 1-4, 6, 8-12, 14-16, 18-28 and 30-31 were rejected under 35 U.S.C. § 102(b) as being anticipated by Sukegawa et al. (U.S. Patent No. 5,603,001). Applicant respectfully traverses.

Claims 1, 14, and 19, as currently amended, each recite a memory device controller having an updateable register bank adapted to send a first signal to an analog/memory core of the memory device for controlling operation of the analog/memory core; a bus controller coupled to the register bank, the bus controller adapted to receive a second signal from the register bank and to send a third signal to the register bank for updating the register bank; a select register coupled to the register bank; and a processor coupled to the bus controller and the select register; wherein the first signal is sent from the register bank to the analog/memory core without passing through the bus controller.

For Robinson, the Examiner has taken an interface 30 for a flash memory device 27 (Figure 3) as corresponding to the memory device controller of claim 1, 14, or 19, a central processing unit ("CPU") 11 of a computer system 10 (Figure 1) as corresponding to the processor of claim 1, 14, or 19, and a bridge circuit 14 of computer system 10 (Figure 1) as corresponding to the bus controller of claim 1, 14, or 19. This is different than claim 1, 14, or 19 in that in claim 1, 14, or 19, the processor and bus controller are elements of the memory device controller, whereas Figure 1 shows processing unit ("CPU") 11 and bridge circuit 14 as being separate from and external to a flash memory device array 18. Moreover, there is no indication in Robinson that interface 30 includes processing unit ("CPU") 11 and bridge circuit 14. The Examiner has taken registers 32-58 (Figure 3) as corresponding to the updateable register bank of claim 1, 14, or 19 and a signal from address decode circuit 63 (Figure 3) as corresponding to the first signal of claim 1, 14, or 19. However, address decode circuit 63 is not part of registers 32-58. This is different than claim 1, 14, or 19 in that claims 1, 14, and 19 each recite that the register bank is adapted to send the first signal. Therefore, Robinson does not include each and every recitation of claim 1, 14, or 19, so claims 1, 14, and 19 should be allowed over Robinson.

For Sukegawa et al., the Examiner has taken registers 171-178 of external bus interface 17 (Figure 2) as corresponding to the updateable register bank of claim 1, 14, or 19, an address signal from address conversion table 132 (Figure 2) as corresponding to the first signal of claim 1, 14, or 19, a processor bus interface 15a (Figure 2) and a NAND bus interface 19 (Figure 2) as corresponding to the bus controller of claim 1, 14, or 19, and flash EEPROMs 11-1 to 11-16 (Figure 2) as corresponding to the analog/memory core of claim 1, 14, or 19. However, as shown in Figure 2, an address signal from address conversion table 132 is required to pass through NAND bus interface 19 before arriving at flash EEPROMs 11-1 to 11-16. This is different than claim 1, 14, or 19 in that claims 1, 14, and 19 each recite that the first signal is sent from the register bank to the analog/memory core without passing through the bus controller. Therefore, Sukegawa et al. does not include each and every recitation of claim 1, 14, or 19, so claims 1, 14, and 19 should be allowed over Sukegawa et al.

Claims 2-4 and 6-10 depend from claim 1 and are thus allowable for at least the same reasons as claim 1. Claims 15-17 depend from claim 14 and are thus allowable for at least the same reasons as claim 14. Claims 20-23 depend from claim 19 and are thus allowable for at

least the same reasons as claim 19. Therefore, claims 2-4, 6-10, 15-17, and 20-23 should be allowed.

Claims 11 and 18 each recite a memory device controller having an updateable register bank adapted to send a first signal to an analog/memory core of the memory device for controlling operation of the analog/memory core; a bus controller coupled to the register bank, the bus controller adapted to receive a second signal from the register bank and send a third signal to the register bank for updating the register bank; a select register coupled to the register bank; a first processor coupled to the bus controller and the select register; an expression checker coupled between the first processor and the bus controller; and a transfer register coupled to the bus controller for receiving the third signal therefrom during a first clock phase, and coupled to the register bank for transmitting the third signal thereto during a second clock phase.

For Robinson, the Examiner has taken an interface 30 for a flash memory device 27 of (Figure 3) as corresponding to the memory device controller of claim 11 or 18, a central processing unit ("CPU") 11 of a computer system 10 (Figure 1) as corresponding to the first processor of claim 11 or 18, and a bridge circuit 14 of computer system 10 (Figure 1) as corresponding to the bus controller of claim 11 or 18. This is different than claim 11 or 18 in that in claim 11 or 18, the first processor and bus controller are elements of the memory device controller, whereas Figure 1 shows processing unit ("CPU") 11 and bridge circuit 14 as being separate from and external to a flash memory device array 18. Moreover, there is no indication in Robinson that interface 30 includes processing unit ("CPU") 11 and bridge circuit 14. The Examiner has taken registers 32-58 (Figure 3) as corresponding to the updateable register bank of claim 11 or 18 and a signal from address decode circuit 63 (Figure 3) as corresponding to the first signal of claim 11 or 18. However, address decode circuit 63 is not part of registers 32-58. This is different than claim 11 or 18 in that claims 11 and 18 each recite that the register bank is adapted to send the first signal. Therefore, Robinson does not include each and every recitation of claim 11 or 18, so claims 11 and 18 should be allowed over Robinson.

For Sukegawa et al., the Examiner has taken registers 171-178 of external bus interface 17 (Figure 2) as corresponding to the updateable register bank of claim 11 or 18, a processor bus interface 15a (Figure 2) and a NAND bus interface 19 (Figure 2) as corresponding to the bus controller of claim 11 or 18, a microprocessor (MPU) 15 (Figure 2) as corresponding to the first

processor of claim 11 or 18, an ECC calculating circuit 21 (Figure 2) of NAND bus interface 19 as corresponding to the expression checker of claim 11 or 18, a status register 177 of the registers 171-178 of external bus interface 17 as corresponding to the transfer register of claim 11 or 18, and flash EEPROMs 11-1 to 11-16 (Figure 2) as corresponding to the analog/memory core of claim 11 or 18. As shown in Figure 2, the ECC calculating circuit 21 is contained within and is a part of the NAND bus interface 19 that the Examiner has taken as corresponding in part to the bus controller of claim 11 or 18. This is different than claim 11 or 18 in that the expression checker of claim 11 or 18 is coupled between the first processor and the bus controller, meaning that the expression checker is separate from and lies outside of the bus controller. Further shown in Figure 2 is that status register 177 is one the registers 171-178 that the Examiner has taken as corresponding to the updateable register bank of claim 11 or 18. This is different than claim 11 or 18 in that the transfer register of claim 11 or 18 is coupled to the register bank, meaning that the transfer register is separate from and is not one of the registers of the register bank. Therefore, Sukegawa et al. does not include each and every recitation of claim 11 or 18, so claims 11 and 18 should be allowed over Sukegawa et al.

Claims 12-13 depend from claim 11 and are thus allowable for at least the same reasons as claim 11. Therefore, claims 12-13 should be allowed.

Claim 24, as currently amended, recites that the control signal is sent from the third register of the register bank to the analog/memory core without passing through the bus controller. For Sukegawa et al., the Examiner has taken registers 171-178 of external bus interface 17 (Figure 2) as corresponding to the register bank of claim 24, a NAND bus interface 19 (Figure 2) as corresponding to the bus controller of claim 24, flash EEPROMs 11-1 to 11-16 (Figure 2) as corresponding to the analog/memory core of claim 24, and a signal from error register 178 as corresponding to the control signal of claim 24. However, as shown in Figure 2, signals from registers 171-178 of external bus interface 17 are required to pass through NAND bus interface 19 before arriving at flash EEPROMs 11-1 to 11-16. This is different than claim 24 in that claim 24 recites that the control signal is sent from the third register of the register bank to the analog/memory core without passing through the bus controller. Therefore, Sukegawa et al. does not include each and every recitation of claim 24, so claim 24 should be allowed.

Claims 25-28 and 30-31 depend from claim 24 and are thus allowable for at least the same reasons as claim 24. Therefore, claims 25-28 and 30-31 should be allowed.

Claim Rejections Under 35 U.S.C. § 103

Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Robinson. Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Sukegawa et al.

Claim 1 is patentably distinct from Robinson and from Sukegawa et al. The taking of Official Notice that Robinson teaches that data may be sent to register 28 (Figure 3) and be clocked serially in a preordered sequence so that it may be read on a bus 12 (Figure 1) by a processor fails to overcome the deficiencies of Robinson with regard to claim 1. The taking of Official Notice that Figures 18A-18G, 20A-20G, 22A-22G, and 25A-25B of Sukegawa et al. illustrate a timing sequence of events according to phases of a clock, which implies that a series of clocks are used to facilitate operations fails to overcome the deficiencies of Sukegawa et al. with regard to claim 1. Claim 5 depends from claim 1 and is thus allowable for at least the same reasons as claim 1. Therefore, claim 5 should be allowed.

CONCLUSION

In view of the above remarks, Applicant believes that all pending claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. Please charge any further fees deemed necessary or credit any overpayment to Deposit Account No. 501373.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2208.

Respectfully submitted,

Date: 07-20-06

Tod A. Myrum
Reg. No. 42,922

Attorneys for Applicant
Leffert Jay & Polglaze
P.O. Box 581009
Minneapolis, MN 55458-1009
T (612) 312-2200
F (612) 312-2250